



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,732	05/27/2005	Eric Desmicht	FR02 0129 US	4315

65913 7590 08/05/2009  
NXP, B.V.  
NXP INTELLECTUAL PROPERTY & LICENSING  
M/S41-SJ  
1109 MCKAY DRIVE  
SAN JOSE, CA 95131

EXAMINER
----------

OKEKE, IZUNNA

ART UNIT	PAPER NUMBER
----------	--------------

2432

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/05/2009

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/536,732	<b>Applicant(s)</b> DESMICHT ET AL.	
	<b>Examiner</b> IZUNNA OKEKE	<b>Art Unit</b> 2432	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,3 and 5-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3 and 5-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed 06/06/2009 have been fully considered but they are not persuasive.

On Pages 1 and 2 of applicant's argument and remarks, applicant argues that Moller does not teach the protected data activating or deactivating an optional feature of the chip. In making the argument, applicant wrongly characterized Moller's protection data and protected data with the assertion that the data interface enabling/disabling data of Moller is the protection data and not the protected data. The 1 and 0 bits which enable and disable the external interface in Moller's invention are not the protection data but are part of the protected data in the PCR. A distinction is hereby presented of Moller's protected and protection data. In Para 25 and 27, Moller describes the protection data (Key 1, Key 2) which are passwords which must be present for the decryption of the protected data. Moller describes the protected data in Para 24 and 28, the protected data located in the 2<sup>nd</sup> memory portion (user area) which comprises the PCR containing the enable and disable data (1 and 0 bits) for enabling or disabling a data interface which a feature of the chip. As disclosed by Moller and as interpreted by the examiner, the protection data is (Key 1, Key 2) for protecting access to the data and the protected data are encrypted user programs or the 1 and 0 enable/disable bits stored in the PCR for enabling or disabling a feature of the chip.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 5 and 6-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Moller et al. (US-20030014653).

a. Referring to claim 1 and 9:

Regarding claim 1 and similar claim 9, Moller teaches a chip for processing a content, comprising at least a microprocessor, characterized in that said chip includes an integrated non-volatile programmable memory & restoring for storing protection data and protected data, said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed (See the response to argument and Para 6-7 and 24-28 teaches a chip for processing a content, the chip comprises a microprocessor and non-volatile memory for storing protection data for authorizing/denying access to protected data), wherein said protection data is only modifiable so as to increase the said protection level and said protected data includes data to activate/deactivate an optional feature of the chip (Para 24, 25 and 27-28.... Protection data (Passwords Key 1 and Key 2) modifiable to increase the access protection level and the protected data stored in the PCR (1 and

Art Unit: 2432

0 bits) used in enabling/disabling a feature of the chip).

a. Referring to claim 3:

Regarding claim 3, Moller teaches a chip according to Claim 1, wherein said protection data includes a password, said access being authorized/denied through a password check (Para 10 teaches the protection data including a password or keyword and access being authorized or denied thru a password check)..

a. Referring to claim 5:

Regarding claim 5, Moller teaches a chip according to Claim 1, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device (Para 12 teaches the optional feature as a connection to external data devices through the external data interfaces).

a. Referring to claim 6:

Regarding claim 6, Moller teaches a chip according to Claim 1, wherein said protected data includes data to activate/deactivate an external boot program for said microprocessor, said external boot program including instructions for downloading a new boot program for said microprocessor from an external memory (Para 12 teaches a PCR register in the memory block containing protected data which include data to activate/deactivate external data interfaces for downloading or modifying or debugging an initialization or boot program).

a. Referring to claim 7:

Regarding claim 7, Moller teaches a chip according to Claim 1, wherein said protection data includes a value defining an address limit from which the data stored at said memory are

Art Unit: 2432

protected data and access to such protected data is denied (Para 24 teaches a defined address limit for the protected data and access is denied).

a. Referring to claim 8:

Regarding claim 8, Moller teaches a chip according to Claim 7, wherein said protected data include includes programs and data operating a conditional-access dedicated microprocessor (See Moller, Para 3-4 teaches an encryption – decryption program for operating a conditional access processor wherein the program decrypts and provides the content to the user).

a. Referring to claim 10:

Regarding claim 10, Moller teaches a device as claimed in Claim 9, wherein the device is intended to process encrypted video/audio data (See Para 9).

a. Referring to claim 11:

Regarding claim 11, Moller teaches a method for obtaining a protected chip including at least a microprocessor, said method using a chip, said method including:

using at least an authorized access to modify protected data in an integrated non-volatile memory (See Moller, Para 12, Line 17-20 teaches using an authorized access to modify protected data),

protecting the access to said protected data in said integrated non-volatile memory by modifying protection data in order to deny said access (See Moller, Para 25 teaches modifying the protection data to protect access to the protected data), wherein said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed, wherein-said protection data is only modifiable so

Art Unit: 2432

as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip (See the rejection in claim 1)

a. Referring to claim 12:

Regarding claim 12, Moller teaches a chip according to Claim 1 further comprising a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor (Fig 5 and Para 6... instruction set of microprocessor coupled between memory and processor connection bus).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (US-20030014653), and further in view of Boyle et al. (US-6118870).

a. Referring to claim 13:

Regarding claim 13, Moller teaches a chip according to claim 1. Moller does not explicitly teach the chip having a MIPS instruction set. However, Boyle teaches a chip having a MIPS instruction set (See Boyle, Col 10, Line 3-18). Therefore it would have been obvious to one of ordinary skill to implement Moller's chip as a microprocessor having a MIPS instruction set for the benefit of utilizing RISC architecture which provides higher performance by making instruction execute quickly and is designed for use with high level programming languages.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IZUNNA OKEKE whose telephone number is (571)270-3854. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 2432

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/I. O./

Examiner, Art Unit 2432

/Jung Kim/

Primary Examiner, AU 2432